AMENDMENTS TO THE CLAIMS

This listing of claims will replace all previous versions and listings of claims in the application.

1. (Currently Amended) A decoding unit for decoding a received signal comprising:

a plurality of soft-decoders, each soft-decoder operable to sample ~~sampling~~ the received signal at a different time within a symbol period and to output ~~outputting~~ two values for each sample, the first value comprising a preliminary decoded value and the second value comprising an ambiguity indicator; and

a logic device coupled to the each of the soft-decoders, for determining a decoded value for each symbol based on one or more preliminary decoded values and ambiguity indicators.

2. (Currently Amended) The decoding unit of Claim 1, wherein ~~each of~~ the soft-decoders are substantially identical to one another.

3. (Original) The decoding unit of Claim 1, wherein each soft-decoder comprises:

a first comparator with inputs comprising the received signal and a first reference voltage;

a second comparator with inputs comprising the received signal and a second reference voltage; and

a third comparator with inputs comprising the received signal and a third reference voltage.

4. (Original) The decoding unit of Claim 1, wherein each soft-decoder comprises a plurality of comparators and one or more logical AND gates.

5. (Original) The decoding unit of Claim 1, further comprising a plurality of delay elements coupled to the soft-decoders.

6. (Original) The decoding unit of Claim 1, further comprising a plurality of delay elements coupled to the soft-decoders, each delay element delaying the received signal by a different amount.

7. (Currently Amended) The decoding unit of Claim 1, further comprising a plurality of delay elements coupled to the soft-decoders, each delay element delaying [[the]] a clock signal by a different amount.

8. (Currently Amended) A decoding unit for decoding a received signal comprising:

an asynchronous soft-decoder that continuously samples the received signal and produces a decoded output signal and an ambiguous indicator signal;

a plurality of first delay elements coupled to a first soft-decoder, each first delay element generating a different delay relative to another first delay element and producing an [[first]] ambiguity indicator from the ambiguous indicator signal;

a plurality of second delay elements coupled to a second soft-decoder output, each second delay element generating a different delay relative to another second delay element and producing a preliminary decoded output from the decoded output signal; and

a logic device coupled to the each of the first and second delay elements, for determining a decoded value based on one or more of the preliminary decoded outputs and ambiguity indicators.

9. (Original) The decoding unit of Claim 8, wherein the soft-decoder comprises:

a first comparator with inputs comprising the received signal and a first reference voltage;

a second comparator with inputs comprising the received signal and a second reference voltage; and

a third comparator with inputs comprising the received signal and a third reference voltage.

10. (Original) The decoding unit of Claim 8, wherein the soft-decoder comprises a plurality of comparators and one or more logical AND gates.

11. (Currently Amended) A decoding unit for decoding a received signal comprising:

an analog-to-digital converter for sampling the received signal faster than once every symbol period of the received signal and outputting for each sample a first value comprising a preliminary decoded value and a second value comprising an ambiguity indicator;

a processor coupled to the converter for grouping a subset of sampled first and second values derived from the single symbol period, for examining the subset of sampled first and second values and determining a first value closest to an optimum sampling time based on a principle of generalized maximum likelihood, for decoding the first value closest to the optimum sampling time and outputting that ~~sample~~ decoded first value as the decoded symbol.

12. (Original) The decoding unit of Claim 11, further comprising a clock recovery unit coupled to the converter for providing a clock signal.

13. (Currently Amended) The decoding unit of Claim 11, wherein the processor calculates the first value closest to the optimum sampling time by:

computing an absolute difference between each first value and a nearest level corresponding to a decoded symbol;

finding a first value which has a smallest absolute difference from the subset of first values; and

taking the ~~sample~~ first value with the smallest absolute difference as the ~~sample~~ first value closest to the optimum sampling time.

14. (Currently Amended) A method for decoding a received signal comprising:

receiving a signal;

estimating an optimal timing offset on a symbol-by-symbol basis; and

decoding the ~~communicated~~ received signal using generalized maximum likelihood estimation with the estimated optimal timing offset.

15. (Original) The method of Claim 14, wherein estimating an optimal timing offset on a symbol-by-symbol basis further comprises generating an ambiguity indicator and a preliminary decoded value for a sample.

16. (Currently Amended) The method of Claim 14, wherein estimating an optimal timing offset on a symbol-by-symbol basis further comprises:

dividing the received signal into a plurality of received signals; and

delaying each of the ~~one or more~~ plurality of received signals by different amounts of time.

17. (Original) The method of Claim 14, wherein estimating an optimal timing offset on a symbol-by-symbol basis further comprises:

dividing an ambiguity indicator signal and a preliminary decoded value signal derived from the received signal; and

delaying each ambiguity indicator signal and each preliminary decoded value signal by different amounts of time.

18. (Original) The method of Claim 14, wherein estimating an optimal timing offset on a symbol-by-symbol basis further comprises:

determining a clock signal from the received signal;

taking multiple samples of the received signal in accordance with the clock signal; and

converting the received signal into the digital domain based on the multiple samples.

19. (Currently Amended) The method of Claim 14, wherein decoding the received signal using generalized maximum likelihood estimation with [[an]] the optimal ~~sampling point~~ timing offset further comprises determining a sample timing index from one or more ambiguity indicators.

20. (Currently Amended) The method of Claim 14, wherein decoding the received signal using generalized maximum likelihood estimation with [[an]] the optimal ~~sampling point~~ timing offset further comprises identifying a symbol that corresponds to a selected timing index.